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A new topology of fuel cell hybrid power source for efficient operation and high reliability

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ABSTRACT

This paper analyzes a new fuel cell Hybrid Power Source (HPS) topology having the feature to mitigate the current ripple of the fuel cell inverter system. In the operation of the inverter system that is grid connected or supplies AC motors in vehicle application, the current ripple normally appears at the DC port of the fuel cell HPS. Consequently, if mitigation measures are not applied, this ripple is back propagated to the fuel cell stack. Other features of the proposed fuel cell HPS are the Maximum Power Point (MPP) tracking, high reliability in operation under sharp power pulses and improved energy efficiency in high power applications. This topology uses an inverter system directly powered from the appropriate fuel cell stack and a controlled buck current source as low power source used for ripple mitigation. The low frequency ripple mitigation is based on active control. The anti-ripple current is injected in HPS output node and this has the LF power spectrum almost the same with the inverter ripple. Consequently, the fuel cell current ripple is mitigated by the designed active control. The ripple mitigation performances are evaluated by indicators that are defined to measure the mitigation ratio of the low frequency harmonics. In this paper it is shown that good performances are obtained by using the hysteretic current control, but better if a dedicated nonlinear controller is used. Two ways to design the nonlinear control law are proposed. First is based on simulation trials that help to draw the characteristic of ripple mitigation ratio vs. fuel cell current ripple. The second is based on Fuzzy Logic Controller (FLC). The ripple factor is up to 1% in both cases.

1. Introduction

The Polymer Electrolyte Membrane Fuel Cell (PEMFC) stack represents one of the most used solutions as main energy source in Energy Generation System (EGS) and vehicle applications because of its small size, the ease of construction, a fast start-up and low operating temperature. Unfortunately, its relatively short life represents yet an impediment to their commercialization [1]. As it is known, the inverter current ripple is the main factor responsible for low performance regarding the PEMFC energy efficiency [2–5] and PEMFC life cycle [6–9]. Also, it is known that low frequency (LF) spectral components of the PEMFC current ripple affect in much measure the PEMFC life cycle than high frequency (HF) spectral components. LF current spectral components cause hysteretic losses and subsequently more fuel consumption. LF current spectral components contribute with up to 10% reduction in the available output power [10], so some restrictions for spectral components of the fuel cell (FC) current ripple are specified. It is known that PEMFC is highly intolerant to LF current ripple or other slow variations of the load power. The equivalent electrical model of the PEMFC has a rather large capacitance shunting the device, which mitigates the current ripple, but with a degradation of its performance. Also, this suggests that the fuel cell can in-fact tolerate high frequency (HF) current ripple. The limits of the PEMFC current ripple were given for first time by the USA National Energy Technology Laboratory (NETL) [11] as below:

- 100/120 Hz ripple < 15% from 10% to 100% load, not to exceed 0.6 A for lighter loads;
- 50/60 Hz ripple < 10% from 10% to 100% load, not to exceed 0.4 A for lighter loads;
- 10 kHz and above < 60% from 10% to 100% load, not to exceed 2.4 A for lighter loads;
- in range >100/120 Hz to <10 kHz the ripple limit is a value linearly interpolated between the 120 Hz and 10 kHz limits.

The LF inverter current ripple reduces with more than 10% the maximum output power, so it must be mitigated under the new reliability limits that are specified by the Ripple Factor (RF):

$$\mathrm{RF}_I = \frac{I_{\mathrm{Max}} - I_{\mathrm{Min}}}{I_{(\mathrm{AV})}} \quad (1)$$

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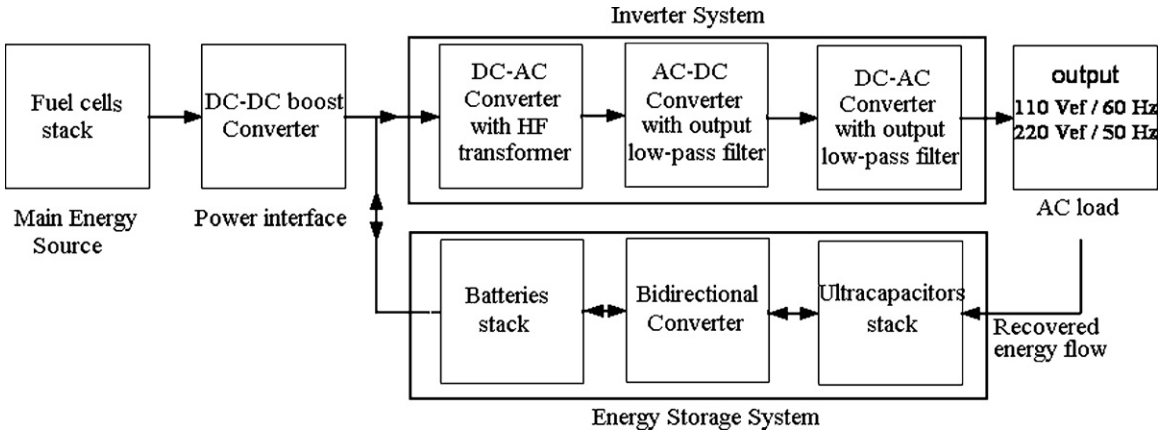


Fig. 1. Basic EGS topology with the inverter system powered by a FC stack.

where I_{Max}, I_{Min}, and $I_{(AV)}$ are the value of maximum, minimum and average, respectively.

For example, LF RF must be up to 5% and HF RF must be up to 40%, but, obviously, lower values for RF are recommended to increase PEMFC performances [12]. The interleaved technique that is used in parallel power converters can be a solution [13,14].

In FC EGS applications, variations of the load power below 50/60 Hz represent "load following" action of the EGS control and power flow supplied by PEMFC power is also changing if only the PEMFC stack is used as energy source. The PEMFC control should track to within 1% the Maximum Power Point (MPP) of PEMFC stack for purposes of both integrity and efficiency of it [15–17]. Consequently, the MPP tracking solution is used in proposed FC HPS topology.

In FC vehicle applications, high energy demands can appear for a short time. These power peaks will cause high slopes of PEMFC current and, subsequently, the voltage drops appear. So, to avoid this phenomenon of fuel starvation, it is necessary to add Energy Storage Devices (ESD) on FC vehicles [18–20]. Obviously, using of the ESD is also needed in FC EGS under dynamic load to assure the power balance, taking in account the response time of ESDs used. Usually, batteries and ultracapacitors are used as ESDs. These devices are also required to absorb the energy from the regenerative braking or other recovered power flows and to compensate the power peaks of load. The control of power flows determines the batteries and ultracapacitors stacks to supply such sharp power peaks, improving the reliability of PEMFC stack [20,21]. The current slopes are given experimentally for different PEMFC stacks, depending on their power (about 10 A s^{-1} per each kW power) [5,22,23]. So, it is obvious that ESD and FC technologies need to be merged in Hybrid Power Sources (HPS). Usually, a HPS combines one or more energy sources with mixed ESDs that operate together to deliver power (to the DC load or into the AC grid via the inverter system) or to store energy. The use of a mixed ESD stack of ultracapacitors and batteries permits reduction of the hydrogen consumption and a reliable FC HPS operating under sharp power pulses [24,25]. Consequently, this solution is also used in proposed FC HPS topology.

The challenge for control of power flows in FC HPS is to enhance all performance indicators through its technologies that working together [26]. As it is mention above, the RF of PEMFC current is one of main performance indicators of FC HPS. The power interfaces used to mitigate the ripple of inverter current and its associate ripple models are analyzed in [27–29]. Ref. [27] presents some aspect of PEMFC ripple modeling, showing some problems of unexpected behavior of ripple model presented in [29].

The proposed FC HPS structure has a control loop for ripple mitigation. The control goal is the mitigation of the inverter current ripple as much as possible by optimal designing of the control law.

The remainder of the paper is organized as follows. Section 2 present state-of-the-art FC HPS topologies. In Section 3 is presented the proposed FC HPS topology with current ripple mitigation control. The issue of estimation of the ripple levels in different FC inverter systems is presented in Section 4. These results are used in designing of an equivalent load that can replace the FC inverter systems in simulation in order to show the mitigation process much better. The proposed FC HPS topology is modeled in Section 5. Simulation results are shown in Section 6 for case of use a hysteretic control. Designing of the nonlinear law used in mitigation control loop is shown in Section 7. Simulation results shown in this section are based on implementation of the nonlinear law by a piecewise linear (PWL). The possibility to design the PWL nonlinear law by a Fuzzy Logic Controller (FLC) is shown in this section, too. The performance indicators for mitigation of the low frequency harmonics are computed in each case. Last section concludes the paper.

2. State-of-the-art FC HPS topologies

For vehicle applications have already reported some HPS structures of type FC/ultracapacitor [30], FC/battery [31] and FC/ultracapacitor/battery [12]. Some typical topologies of the fuel cell inverter systems are presented below. Fuel cell current ripple may be mitigated by passive filtering on high-voltage (HV) and low-voltage (LV) DC buses or by an adequate active control that operates at different energy conversion stages. Because passive filters are bulky at high power of load, the second method is usually used. The basic FC EGS topology is presented in Fig. 1.

If the power of AC load is relative constant, then an FC EGS topology without ESDs may be used. If the inverter system is powered directly by the fuel cells stack, then the ESD capacity is reduced or even canceled [1]. The inverter efficiency increases if the stages number of energy conversion should be minimized. A multi-port FC HPS topology using a bi-buck power interface for ripple mitigation is proposed in [32]. The high energy efficiency is obtained for the FC EGS if the PEMFC stack operates close to Maximum Power Point (MPP). The FC HPS topology that operates close to MPP is shown in Fig. 2.

The PEMFC stack (P_{FC}) and ESD stack (P_{ESD}) assure the power flow on LV DC bus via the MPP boost converter (P_1) and bidirectional converter (P_2), respectively. The power balance at HPS output is $P_{load} = P_1 + P_2$, were the load power flow, P_{load}, is given by the inverter system. The power flows management is performed by the MPP controller and LV DC bus controller. The fuel cell MPP current (I_{MPP}) is tracked in an adaptive feedback loop by injecting the probing current [33]. The power ripple becomes lowest when the operation point gets closer to MPP [34].

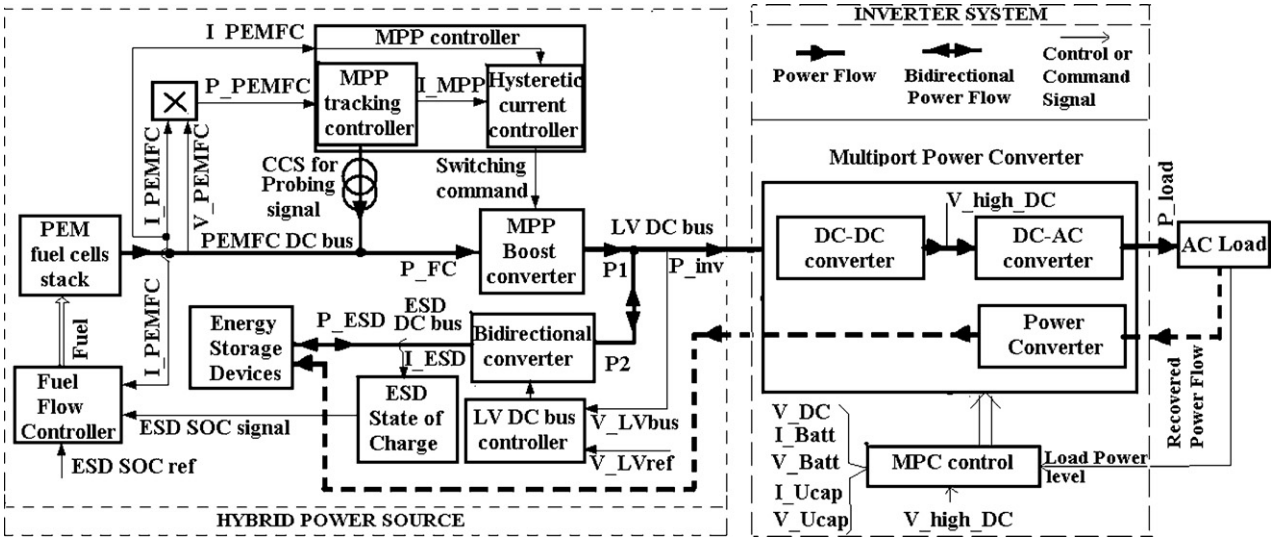


Fig. 2. Hybrid power source topology that operates at MPP of PEMFC stack.

In performed simulations, the load dynamic is simulated by the load sequence. If ESD state of charge (SOC) is in its admissible range, then the fuel flow level is controlled by the fuel cell current. The fuel flow controller assures the fuel rate that is needed to supply the dynamic load. Consequently, the MPP is variable in time. The dynamic of MPP must be tracked by MPP tracking controller in the adaptive feedback loop based on extremum seeking control. The probing signal is generated by a Controlled Current Source (CCS) that is controlled by the MPP tracking controller using the PEMFC power, P_{PEMFC}, as control variable. A sine wave dither signal is used in signal processing by the MPP tracking controller and also it is superimposed over the PEMFC current. The MPP boost converter topology is an appropriate solution, used usually to assure a low PEMFC current ripple, and a hysteretic current controller is simple to be used in generating of the switching command. The current error, $I_{MPP} - I_{PEMFC}$, is used to turn the switch on and off by the hysteretic current controller. Both these controllers form the MPP controller (Fig. 2). When stationary load regime is reached, the fuel flow controller assures a constant fuel rate. For a given load sequence a fuel rate sequence is obtained.

In this paper, the performed analysis will not be focused on control of the FC HPS operating at MPP of the PEMFC stack, so the load and fuel rate sequences are set as constants. Consequently, the MPP converter is removed to clearly highlight the obtained performance in ripple mitigation.

3. Proposed FC HPS topology

Fig. 3 is shown the FC HPS topology that will be analyzed in this paper. Note that ESD delivers power via buck CCS to the DC bus. In this case the power balance is $P_{HPS} = P_{FC} + P_{CCS}$, where $P_{CCS} = \eta_{CCS} P_{ESD}$, and $P_{ESD} = P_{Batt} + P_{Ucap}$. When load require more power than is currently available from the PEMFCs stack, the

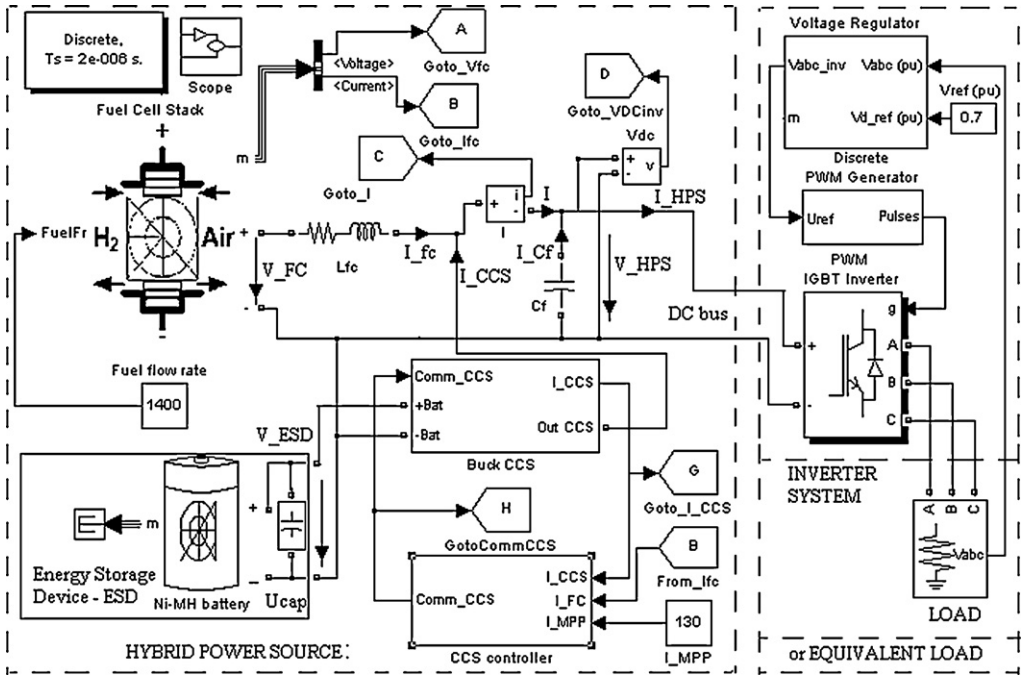


Fig. 3. Proposed hybrid power source topology.

unidirectional converter drains energy from ESD in order to make up the lack.

The architecture without the current ripple mitigation control is also considered in order to compare the obtained results and to show the effectiveness of the mitigation control.

In this paper, the modeling analysis will be focused on designing and operation of the FC HPS with active ripple mitigation based on nonlinear control. This topology is proposed to obtain both performances in energy conversion and ripple mitigation. The FC HPS topology uses an inverter system directly powered from the appropriate fuel cell stack and a buck CCS as low power source supplied by the ESD stack. A FC/ESD HPS structure is considered in this paper and the control goal is to mitigate the inverter current ripple as much as possible by using an active nonlinear control.

4. Power spectrum of the current ripple in FC inverter system

The goal of this section is to analyze the current ripple on HV DC bus for an inverter system and to show its power spectrum. It will be shown for mono-phase inverter system powered by FC HPS that LF harmonics appear on HV DC bus at even multiples of twice of the grid frequency. For three-phase case, it will be shown that LF harmonics appear at multiples of triple of the grid frequency. These results will be used in modeling of an equivalent load on the DC bus of FC HPS that can have LF behavior as such of an inverter system.Current ripple in mono-phase EGS

In this section an analysis of current ripple that is back propagation in a mono-phase full-bridge inverter system is made using a typical EGS topology [35]. Different switching command techniques of mono-phase full-bridge inverter system are considered (see Figs. 4 and 5).

Obviously, the fundamental frequency of the output signals is at a grid frequency (50 Hz) and, as it has been stated before, the fundamental frequency for input signals is twice of the grid frequency. In all cases, the power spectrum has significant LF harmonic frequency of 100 Hz, 200 Hz and 300 Hz with a magnitude that is dependent on the switching command used for inverter control. The LF harmonics number is given by the used switching techniques. Also, the level of LF current harmonics that is back propagated to the

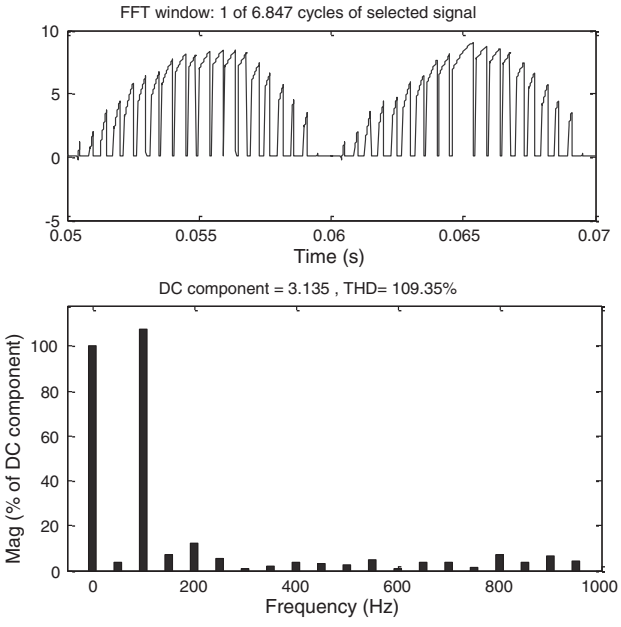


Fig. 4. Current on HV bus of the inverter with pure sine PWM command: signal (top) and its power spectrum (bottom).

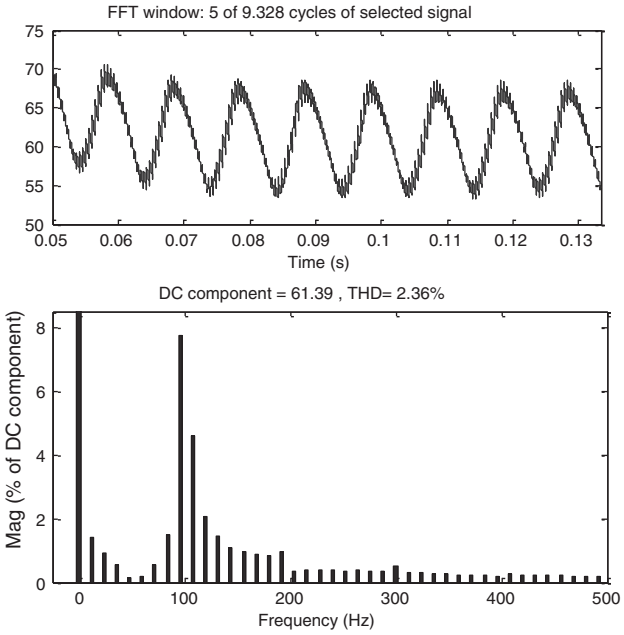


Fig. 5. Current on LV bus of the inverter with modified sine PWM command: signal (top) and its power spectrum (bottom).

PEMFC stack is dependent by the parameters value of the low-pass filters (which are used on LV-side and on HV-side, respectively) in interaction with the impedance of power converters and the PEMFC impedance [3,9,27]. Some aspects will be briefly showed in the next section.Current ripple in three-phase EGS

The goal of this section is to show the current ripple on HV DC bus and its power spectrum for a typical three-phase inverter system (which is adapted after a demo application included in the SimPowerSystem® toolbox). In all simulation cases the AC load parameters for active power, line voltage and frequency are 150 kW, 380 V_{RMS} and 50 Hz, respectively. The LF power spectrum of the input inverter current (Fig. 6) shows the LF current harmonics that are back propagated from the load to the energy source. Obviously, the HF harmonics exist at multiplies of carrier frequency, too. Those HF harmonics were generated by the switching operation of the inverter system (in this case a PWM pure sine command with 10 kHz carrier frequency). Ideally, the power spectrum of a rectified current in a three-phase rectified system with resistive load should be concentrated in the sixth harmonic of the grid frequency (50 Hz). Other LF harmonics can appear as effect of powering of the inverter system. The passive low-pass filter is relatively effective in mitigation of the LF harmonic for a given output impedance of rectified system, but the PEMFC impedance is much different from the output impedance of the rectified system. The current ripple is much more mitigated by the output impedance of the PEMFC stack. In order to see the real value of the inverter ripple it is necessary to estimate the current ripple when an ideal DC voltage source is used (see Fig. 7). The ideal DC voltage source is implemented by a Controlled Voltage Source (CVS). The significant LF harmonics of current on DC bus (which is the input inverter current) are situates at frequency of 150 Hz, 300 Hz and 600 Hz (Fig. 7). This is the ripple of current that affects the PEMFC stack and its main harmonic is situated at triple of the working frequency for the AC load.

So, as a conclusion, the significant LF harmonics are situates in LF frequency band from 100 Hz to 600 Hz.Equivalent load for ripple of current in FC inverter system

As it was showed above, the current on the HV DC bus contains three components: a DC component, a LF component with power spectrum at the grid frequency and its multiples and a HF com-

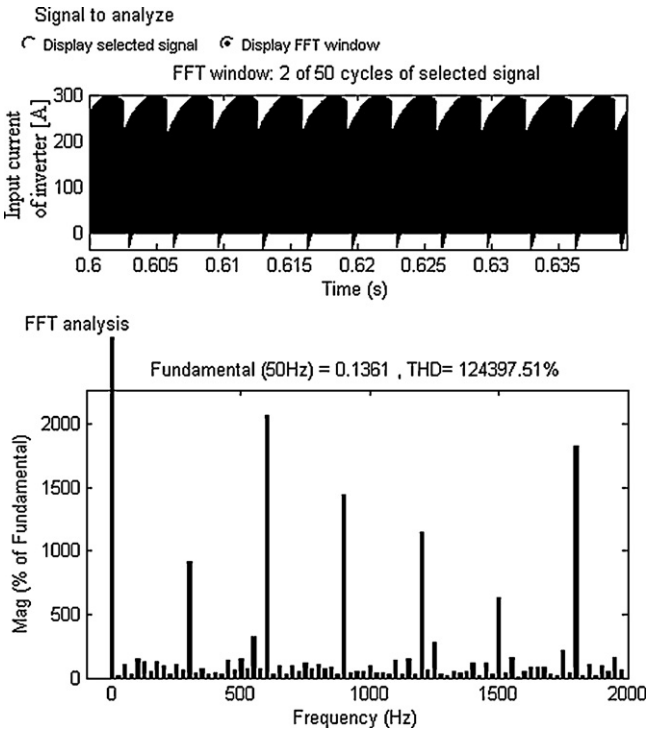


Fig. 6. Input inverter current (top) and its power spectrum (bottom) for the inverter system powered by a rectified grid voltage.

ponent with power spectrum concentrated around the switching frequency of the inverter, f_{sw}, and its multiples.

The levels of HF harmonics are much smaller than LF harmonics levels, so the HF harmonics will not be considering in modeling of the equivalent load that will replace the inverter system. On the other hand, the PEMFC stack has a high tolerant at HF ripple

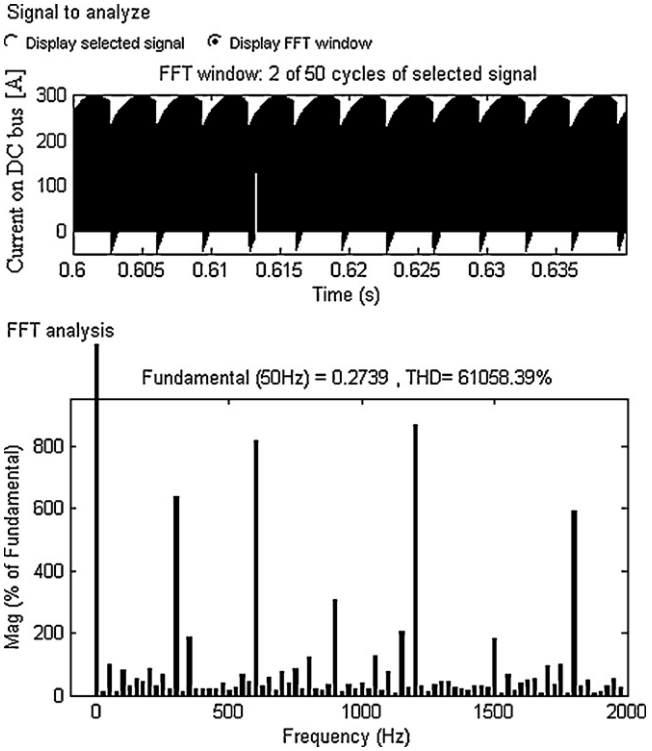


Fig. 7. Input inverter current (top) and its power spectrum (bottom) for the inverter system powered by an ideal DC voltage source.

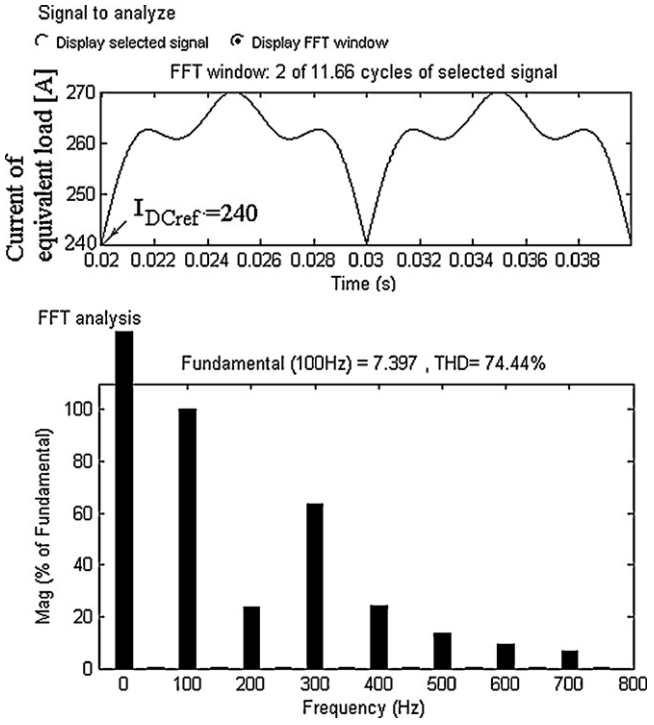


Fig. 8. Current of equivalent load (top) and its power spectrum (bottom).

and the proposed control is for mitigation of the LF ripple. Consequently, only first two components are considered in the model of the equivalent load. The spectral distribution of ripple LF harmonics and observed levels for the input inverter current will be considered in the designing of the equivalent load for inverter system. The equivalent load for the inverter system is implemented by a Controlled Current Source (CCS) having the control signal as a superposition of the three rectified sine waves (with set levels and the frequency of 50 Hz, 150 Hz and 300 Hz) over a DC reference current, I_{DCref}. For example, Fig. 8 is shown the LF power spectrum of the equivalent load using the harmonics level set at 30 A, 5 A and 5 A, respectively. The low-pass filter used for mitigation of HF current ripple is of second order type (L_f = 100 μH and C_f = 10 μF). The DC reference current, I_{DCref}, was chosen in correlation with MPP of the used PEMFC stack (see Fig. 9 that is powered to the maximum fuel flow rate of 1400 lpm (litre per minute). A PEMFC stack of 50 kW/625 V and NiMH batteries stack of 100 Ah/1000 V from the SimPowerSystem® toolbox were used in all simulation. The ultracapacitors stack was modeled by its nominal capacitance (10 F) and series resistance (0.1 Ω).

The reference current is defined as a value slightly smaller than the minimum value of this current and is about 240 A for the equivalent load. The HPS output current, i_{HPS}, is set by the load, so $I_{HPS(ref)}$ = 240 A.

Obviously, the ESD stack current, i_{ESD}, depends of buck CCS efficiency, η_{CCS}. Taking into account that resulting PEMFC current ripple is small, the DC value for the PEMFC current, i_{FC}, can be chosen near to MPP current, I_{MPP}. Consequently, the DC value of ESD stack current can be estimated using the relationships (2):

$$\begin{cases} i_{HPS} = I_{DC(ref)} + i_{load(ripple)} \\ i_{CCS} = I_{CCS(ref)} + i_{CCS(ripple)} \\ i_{FC} = I_{FC(ref)} + i_{FC(ripple)} \\ i_{FC(ripple)} \ll i_{load(ripple)} \\ i_{Cf} \ll i_{HPS} \Rightarrow i_{FC} \cong i_{HPD} - i_{ESD} \end{cases} \Rightarrow \begin{cases} I_{CCS(ref)} \cong \dfrac{\eta_{CCS} V_{ESD(ref)}}{V_{HPS}} \cdot I_{ESD(ref)} \\ I_{FC(ref)} \cong I_{DC(ref)} - I_{CCS(ref)} \\ i_{CCS(ripple)} \cong i_{load(ripple)} \end{cases} \quad (2)$$

Because the current of filtering capacitor, i_{Cf}, is much smaller than load current, the sum of the buck CCS current, i_{CCS}, and the

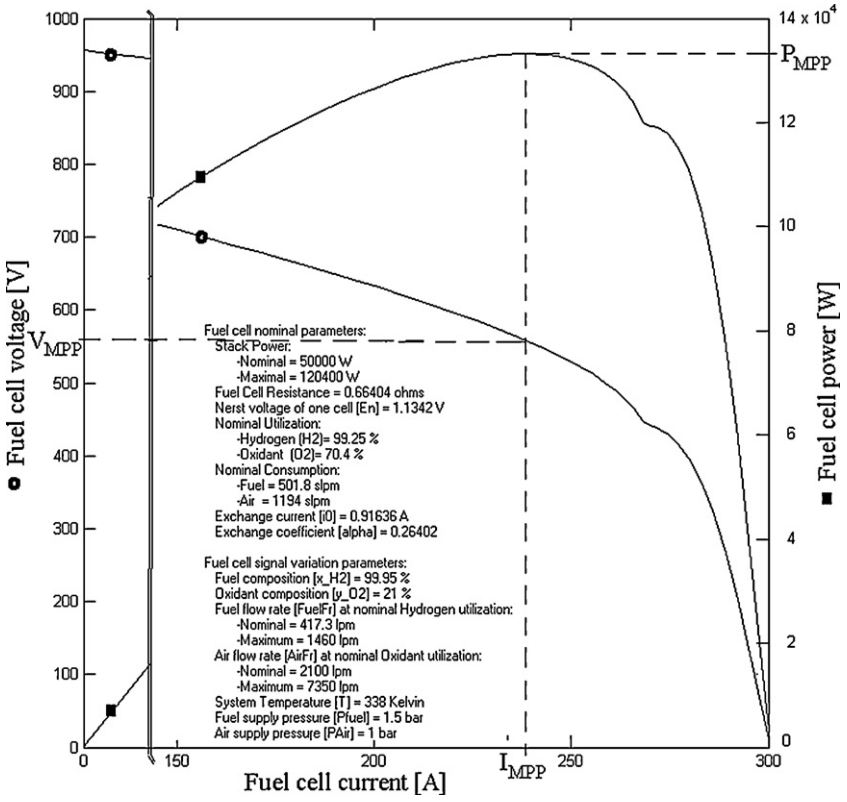


Fig. 9. PEMFC parameters and its static characteristics at maximum fuel flow rate.

PEMFC current, i_{FC}, is almost the HPS current, $i \cong i_{HPS}$. The capacitance of the filtering capacitor can be in range of 1–10 μF for good performance concerning voltage ripple, RF_V. So, if the mitigation loop is active, then ripple of the buck CCS current, $i_{CCS(ripple)}$, is almost equal with the set ripple of load current, $i_{load(ripple)}$ (see last relation of (2)).

The CCS ripple current, $i_{CCS(ripple)}$, is the difference between the time shape of this current and its reference current, so it is positive all the time. Consequently, the unidirectional buck CCS (which is much cheaper than a bidirectional converter) operates well.

The reference current of buck CCS, $I_{CCS(ref)}$, must be set close to zero in order to minimize the energy delivered by the ESD stack. If $I_{CCS(ref)} \cong 0$, then $I_{FC(ref)} \cong I_{DC(ref)} \cong 240\,A \cong I_{MMP}$ and $V_{MPP} \cong 560\,V$ (see Fig. 9).

Considering for ripple of load current only one sine waves (i_s) with frequency, f_s, in LF band, the buck CCS current is:

$$i_{CCS} \cong i_{CCS(ripple)} \cong i_s = I_s|\sin 2\pi f_s t| \tag{3}$$

The average (AV) value of it is:

$$I_{CCS(AV)} \cong I_{CCS(ripple)(AV)} \cong I_{s(AV)} = \frac{2\sqrt{2}}{\pi} I_{s(RMS)} = \frac{I_{s(RMS)}}{K_f} \tag{4}$$

where $K_f \cong 1.11$ is the form factor. Considering for ripple of load current the superposition of sine waves, the average (AV) value of it is:

$$I_{CCS(AV)} = \sum_{s=1}^{\infty} I_{s(AV)} \cong \frac{I_{1(RMS)}}{K_f}\left(1 + \sum_{s=2}^{\infty} \frac{I_{s(RMS)}}{I_{1(RMS)}}\right) \tag{5}$$

The power delivered by the ESD stack is:

$$P_{ESD(AV)} = V_{ESD} I_{ESD(AV)} \cong \frac{V_{MPP} I_{CCS(AV)}}{\eta_{CCS}} \tag{6}$$

The batteries stack parameters were chosen considering the above relationship and load current shown in Fig. 8. The power delivered by the battery stack is about 12 kW, if $\eta_{CCS} \cong 0.9$.

5. Modeling the FC HPS

The proposed FC HPS topology (shown in Fig. 3) is simplified represented in Fig. 10. In this section it will be showed that FC HPS topology can be modeled by a second-order system that uses as state variables the current and voltage on the DC bus. It has been chosen a small inductance ($L_{buck} = L_f = L$) to assure a short time response of buck CCS in tracking process of the inverter current ripple. On the other hand, a lower value than 100 μH will increases the HF ripple over the imposed limits.

Modeling analysis in this section will be focused on current control of the buck CCS. When the control aspects of a system are

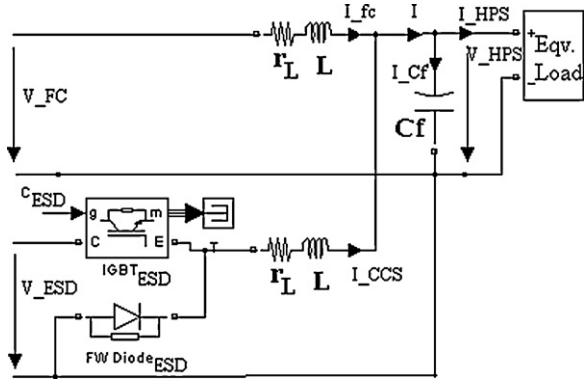


Fig. 10. The FC HPS topology.

studied, the DC components and the LF components are of interest [36].

The switching commands for the IGBT transistor are c_{ESD} (c_{ESD} = 1/0 ⇒ $IGBT_{ESD}$ on/off). Using the above notation, the operating equations are:

$$\begin{aligned} v_{FC} &= r_L i_{FC} + L\frac{di_{FC}}{dt} + v_{HPS} \\ c_{ESD}v_{ESD} &= r_L i_{CCS} + L\frac{di_{CCS}}{dt} + v_{HPS} \\ i_{FC} + i_{CCS} &= i = i_{HPS} + i_{Cf} \cong i_{HPS} \\ v_{HPS} &= r_C i_{Cf} + \frac{1}{C_f}\int i_{Cf}dt \end{aligned} \tag{7}$$

where r_L and r_C are the series resistance of the inductor and the filter capacitor, respectively.

The second-order differential equation of (8) is obtained by summing the first two relations of (7) and then by differentiating the resulted relation:

$$\begin{aligned} \frac{1}{2}(v_{FC} + c_{ESD}v_{ESD}) - v_{HPS} &\cong \frac{r_L}{2}i_{HPS} + \frac{L}{2}\cdot\frac{di_{HPS}}{dt} \Rightarrow 0 \\ &\cong \frac{dv_{HPS}}{dt} + \frac{r_L}{2}\frac{di_{HPS}}{dt} + \frac{L}{2}\frac{d^2 i_{HPS}}{dt^2} \end{aligned} \tag{8}$$

It was considered that $dv_{FC}/dt \cong 0$ and $dv_{ESD}/dt \cong 0$ during this short time of a ripple pulse. If the LF range is considered to be from 100 Hz to 600 Hz, then the time of a ripple pulse will be in range from about 1.6 ms to 10 ms, so, it is much smaller than time constants of the PEMFCs and batteries stacks, which are set to 0.2 s and 10 s, respectively. Relationship (8) gives the behavior of FC HPS output voltage for different shape of the FC HPS output current forced by load.

Neglecting the series resistance r_C, by simple manipulation of the equations of (7), the second-order model of the FC HPS system is written as:

$$\begin{aligned} &\frac{1}{2}(v_{FC} + c_{ESD}v_{ESD}) - \frac{r_L}{2}i_{HPS} - \frac{L}{2}\frac{di_{HPS}}{dt} \\ &= v_{HPS} + \frac{C_f r_L}{2}\frac{dv_{HPS}}{dt} + \frac{C_f L}{2}\frac{d^2 v_{HPS}}{dt^2} \end{aligned} \tag{9}$$

where the second-order system parameters, the natural frequency, ω_n [rad s^{-1}], and the dimensionless damping ratio, ξ, are:

$$\omega_n = \sqrt{\frac{2}{C_f L}}, \quad \xi = \frac{C_f r_L}{4}\omega_n = \frac{r_L\sqrt{2}}{4}\sqrt{\frac{C_f}{L}} \tag{10}$$

This model shows the dependence of FC HPS output voltage to load current, too. Considering a switching frequency of 10 kHz for PWM CCS controller of the buck CCS, the duty cycle of switching command is:

$$D_{ESD} = \frac{t_{onESD}}{T} \cong \frac{V_{MPP}}{V_{ESD}} \cong 0.6 \tag{11}$$

The ripple factor of LF ripple reported to HF ripple, K_{ripple}, is defined as ratio of LF current ripple (peak to peak), $I_{(LF\ ripple)p-p}$, to HF current ripple (peak to peak), $I_{(HF\ ripple)p-p}$:

$$K_{ripple} \triangleq \frac{I_{(LF\,ripple)p-p}}{I_{(HF\,ripple)p-p}} \cong \frac{f_{(HF\,ripple)}}{f_{(LF\,ripple)}} \tag{12}$$

where $f_{(HF\ ripple)} = f_{sw}$ = 10 kHz. Considering LF power spectrum up to 600 Hz ($f_{(LF\ ripple)}$ = 600 Hz), the HF current ripple is of about twenty times lower than LF current ripple.

When $IGBT_{ESD}$ is on, the second equation of (7) is written as:

$$V_{ESD} = L\frac{\Delta i_2}{t_{onESD}} + V_{MPP} \Rightarrow L \cong \frac{V_{MPP}(1 - D_{ESD})T}{I_{(HF\,ripple)p-p}} \tag{13}$$

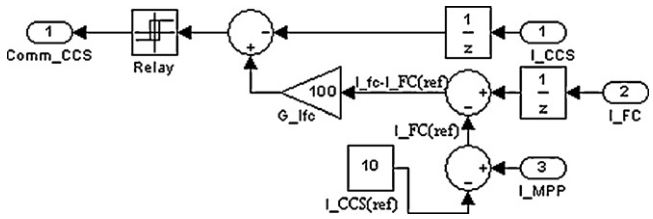


Fig. 11. Structure of CCS hysteretic controller.

The buck CCS inductance value imposes the time constant for tracking of LF load current shape and, therefore, the obtained performance in the mitigation process of the current ripple. For the LF current ripple that is showed in Fig. 8, its value must be lower that:

$$L \cong \frac{V_{MPP}(1 - D_{ESD})K_{ripple}}{f_{sw}\cdot I_{(LF\,ripple)p-p}} \cong 12\times 10^{-3}\ \text{H} \tag{14}$$

As it is known for the PWM voltage control, the output voltage ripple factor is given by:

$$RF_V = \frac{\Delta v_{HPS}}{V_{HPS}} \cong \frac{\pi^2}{2}\cdot(1 - D_{ESW})\cdot\left(\frac{f_n}{f_{sw}}\right)^2, \quad f_n = \frac{\omega_n}{2\pi} \tag{15}$$

If we chose identical inductors, $L_1 = L_2 = L$ = 100 μH, having a series resistance about of r_L = 100 mΩ, and if the output voltage ripple factor is up to 2%, then the filter capacitance, C_f, must be greater that 1 μF. A value of 10 μF is chosen to assure a good ripple factor for FC HPS output voltage (see Fig. 11, where $RF_V \cong 1\%$). If a variable-frequency control method is used, then the switching frequency is designed to be in a range around of 10 kHz value.

Neglecting the series resistor of capacitor, the filtering current amplitude (peak-to-peak) can be estimated by using the last equation of (7):

$$I_{Cf(p-p)} \cong C_f f_{sw} V_{MPP}\cdot RF_V \tag{16}$$

The filtering current amplitude is about of 1.12 A and, therefore, the assumption regarding the filtering current level was correct (see last relation of (2)).

As it is mention before, the voltage of PEMFC and ESD stacks and output voltage of FC HPS can be considered almost constant during of a LF ripple pulse (see also Fig. 13), so:

$$v_{HPS} \cong V_{HPS}, \quad v_{FC} \cong V_{MPP}, \quad v_{ESD} \cong V_{ESD} \tag{17}$$

Because the voltage over the series resistor of L_f inductor (or of C_f inductor, too) is much smaller than output voltage, the first relation of (8) can be rewritten as:

$$\begin{aligned} \frac{1}{2}(v_{FC} + c_{ESD}v_{ESD}) - v_{HPS} &\cong \frac{L}{2}\cdot\frac{di_{HPS}}{dt} \cong \frac{L}{2}\cdot\frac{di_{load(ripple)}}{dt} \\ &\cong \frac{L}{2}\cdot\frac{di_{CCS(ripple)}}{dt} \end{aligned} \tag{8'}$$

This relation can model the HPS behavior in both switching phases of $IGBT_{ESD}$, giving the slope of ripple current.

When mitigation loop is operational (see Fig. 13), the buck CCS generates an anti-ripple current that make an active compensation of the output ripple current, as is shown in relationship (18). In this regime of the HPS operation, the buck CCS behavior is modeled by the second relationship of Eq. (7). Using the same assumptions ($v_{HPS} \cong V_{MPP}$) this relationship can be rewritten as:

$$\frac{c_{ESD}V_{ESD} - V_{MPP}}{L} \cong \frac{di_{CCS}}{dt} \cong \frac{di_{CCS(ripple)}}{dt} \cong \frac{di_{load(ripple)}}{dt} \tag{18}$$

The positive and negative slopes are:

$$s_p \cong \frac{V_{ESD} - V_{MPP}}{L} \cong 4\ \text{A}\,\mu\text{s}^{-1}; \quad s_n \cong \frac{-V_{MPP}}{L} \cong -6\ \text{A}\,\mu\text{s}^{-1} \tag{19}$$

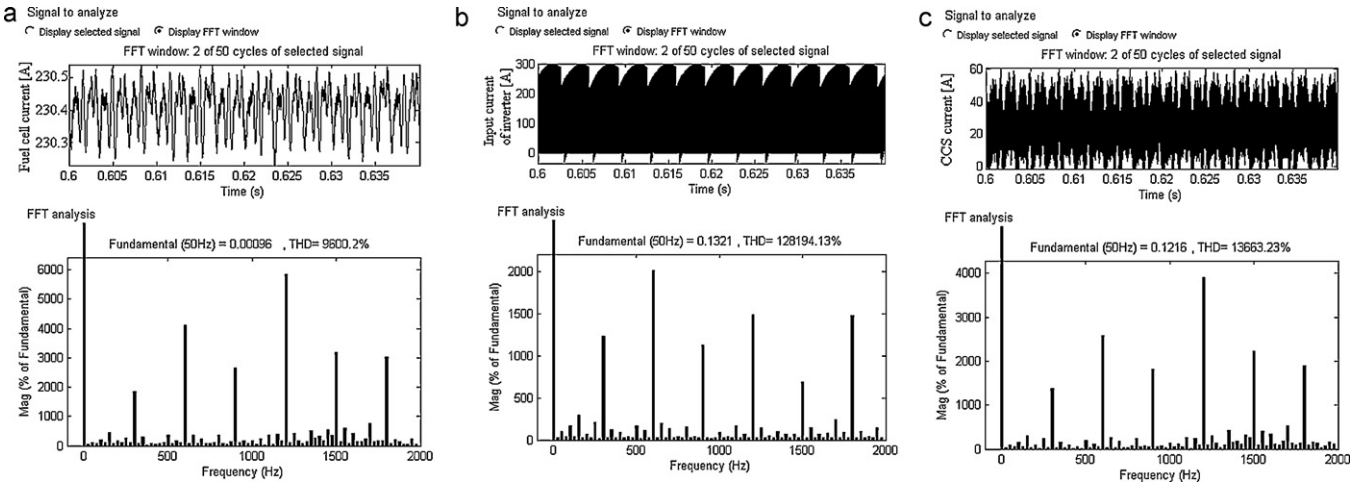


Fig. 12. Simulation results for FC HPS topology with current ripple mitigation control. (a) Fuel cell current ripple (top) and its power spectrum (bottom). (b) Input inverter current (top) and its power spectrum (bottom). (c) Buck CCS current (top) and its power spectrum (bottom).

Table 1
The mitigation ratio for LF harmonics.

Harmonic frequency	300 Hz	600 Hz	900 Hz	1200 Hz	1500 Hz	1800 Hz
MR_H ratio	90	68	57	36	34	69

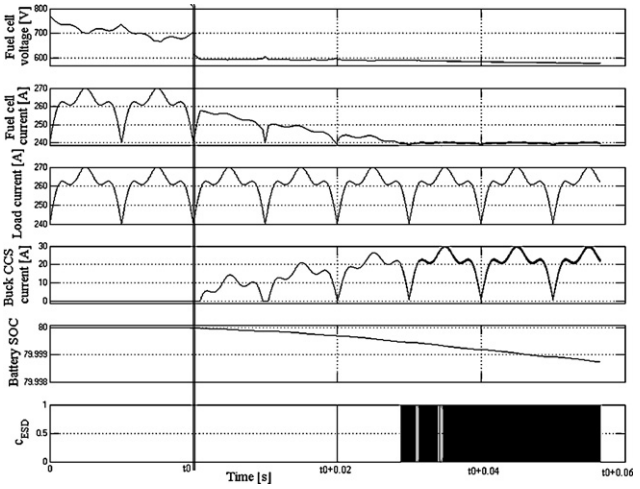


Fig. 13. Behavior of FC HPS topology with current ripple mitigation control that uses an equivalent load.

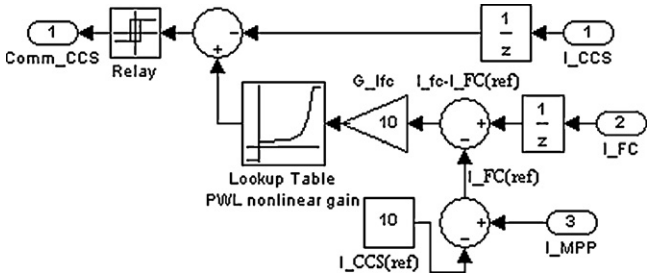


Fig. 15. The CCS nonlinear controller structure.

6. Simulation of FC HPS topology with CCS hysteretic controller

The FC HPS topology with current ripple mitigation control is shown in Fig. 3.CCS hysteretic controller

The hysteretic control was firstly chosen as a control current method, exploiting the simplicity to design it. The structure of CCS hysteretic controller is shown in Fig. 11.

The hysteresis levels were chosen to obtain a HF ripple up to the imposed limits. Tacking 10 A as hysteresis of the relay block, the switching command of buck CCS will be in range of 5–50 kHz. The gain of control loop, G_{Ifc}, set the mitigation level of inverter current ripple by its compensation via the buck CCS current, I_{CCS}. If it is set $I_{CCS(ref)} \cong 10$, then $I_{FC(ref)} \cong 230$ A and $V_{MPP} \cong 600$ V. This will avoid the fuel starvation phenomenon under high peaks of

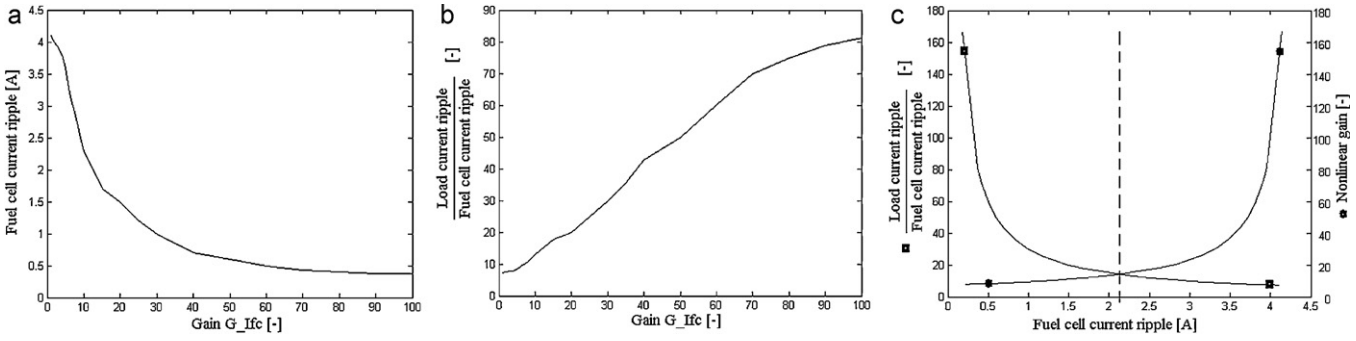
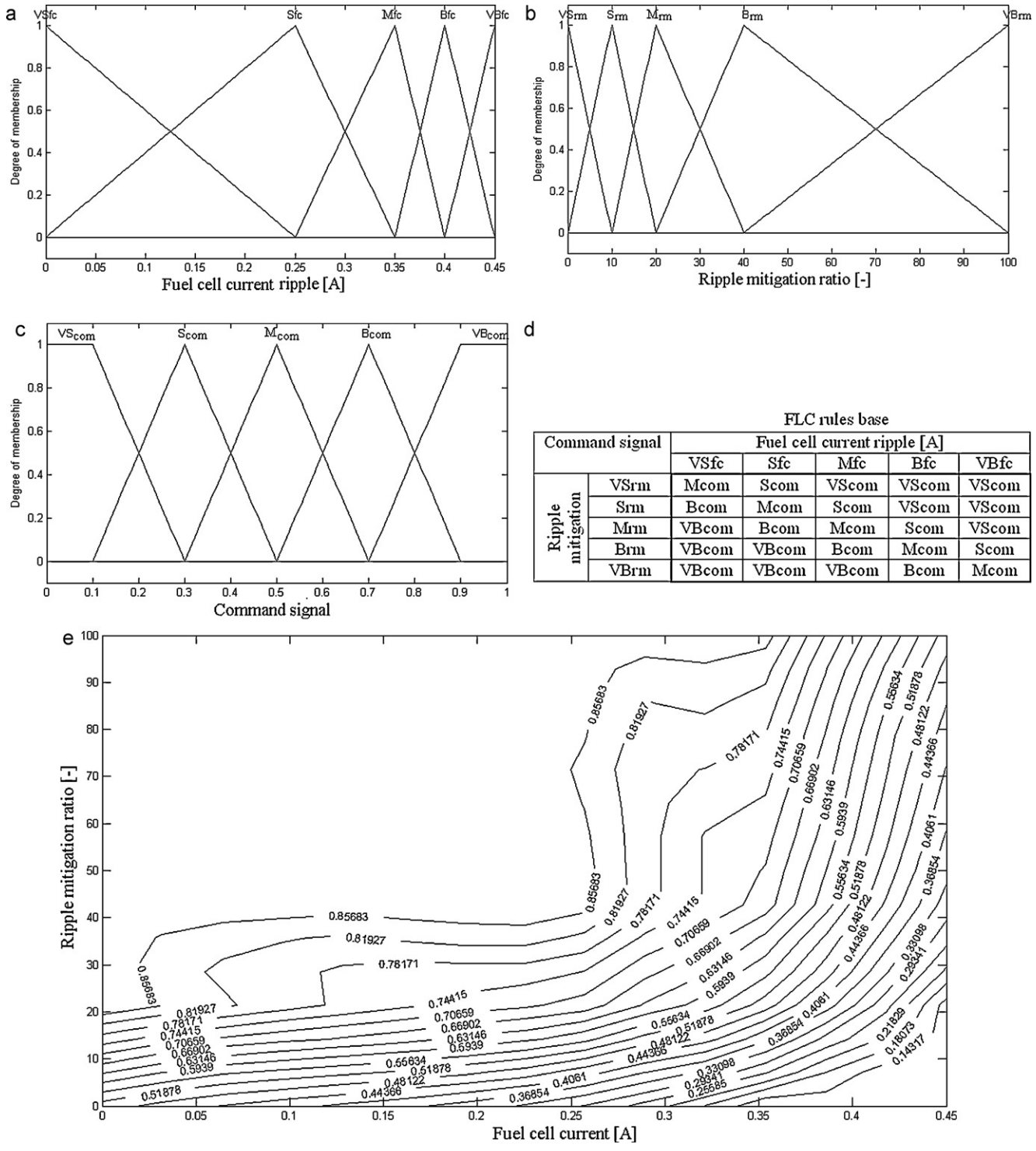


Fig. 14. Performance characteristics of FC HPS topology with current ripple mitigation control. (a) FC current ripple vs. G_{Ifc} gain, (b) MR_H vs. G_{Ifc} gain and (c) MR_H vs. FC current ripple.

load.Simulation results for an FC inverter system powered by FC HPS

The simulation results are shown in Fig. 12 considering the fuel cell EGS architecture with current ripple mitigation control (Fig. 3). It can be observed that the shape of buck CCS current (plot c) tries to track the shape of the fuel cell current (plot a) and this is put in evidence by the levels of LF harmonics, which are almost in the same ratio. Also, it can be observed that the shape of the input inverter current (plot b) is almost the same as those shown before in Figs. 6 and 7. The harmonics mitigation ratio, $MR_H = H_{Inverter}/H_{FC}$, is measured for each harmonic (see plot b and c of Fig. 12), as ratio of harmonic level of the inverter input current to the level of the same harmonic of fuel cell current. The approximate values for MR_H are given in Table 1. The MR_H is of same order of magnitude with the used gain ($G_{Ifc} = 100$) in the loop control. For the fundamental frequency, the mitigation ratio is close to the used gain in all simulation performed for different values of this gain (see next section).



FLC rules base

Command signal		Fuel cell current ripple [A]				
		VSfc	Sfc	Mfc	Bfc	VBfc
Ripple mitigation	VSrm	Mcom	Scom	VScom	VScom	VScom
	Srm	Bcom	Mcom	Scom	VScom	VScom
	Mrm	VBcom	Bcom	Mcom	Scom	VScom
	Brm	VBcom	VBcom	Bcom	Mcom	Scom
	VBrm	VBcom	VBcom	VBcom	Bcom	Mcom

Fig. 16. Designing of FLC and its characteristics. (a) Fuel cell current ripple memberships, (b) Ripple mitigation ratio memberships, (c) Command signal memberships, (d) FLC rules base and (e) Contours of the FLC control surface.

In order to compare the effective mitigation due by the buck CCS, the simulation of the FC HPS topology without current ripple mitigation control is also performed. The effective mitigation ratio (MR_E) is defined for each LF harmonic of fuel cell current as harmonic levels ratio in case without buck CCS and with the buck CCS, respectively. To better highlight the mitigation process by the compensation of the inverter LF current ripple via buck CCS current, in next section, an equivalent load will replace the inverter system.Simulation results for FC HPS that supply an equivalent load

The FC HPS topology with current ripple mitigation control that uses an equivalent load to replace the inverter system is showed in Fig. 3, too. The start-up of mitigation process is shown in Fig. 13.

The MR_H ratio for each LF harmonic was computed by simulation for different G_{Ifc} gain in range 1–100. For example, the MR_H of the 100 Hz harmonic is about 11 and 95 in case of using a G_{Ifc} gain of 10 and 100, respectively. This suggests once again that MR_H ratio is not linear with the frequency of harmonic and its level.

7. Designing of the nonlinear law used in mitigation control loop

Fuel cell current ripple vs. G_{Ifc} gain is shown in Fig. 14a. It can be observed that mitigation of fuel cell current ripple is significantly for G_{Ifc} gain up to 40 and much smaller for G_{Ifc} over to 40. The ripple mitigation ratio, RM_R, is measured as ratio of equivalent load current ripple to fuel cell current ripple, $RM_R = \Delta I_{load}/\Delta I_{FC}$. Using simulation results, the RM_R is shown in Fig. 14b. Its shape is similar with the MR_H shape. These characteristics also show that G_{Ifc} gain must be nonlinear.Designing of nonlinear law by a piecewise linear gain

Ripple mitigation ratio (RM_R) vs. fuel cell current ripple is shown in Fig. 14c (marker ■) considering G_{Ifc} gain values in the extended range up to 200. Ripple mitigation ratio can be almost constant for different load current ripple (or fuel cell current ripple) levels if the nonlinear gain, NG_{Ifc}, (marker ●) is defined symmetrically about the dashed vertical axis. The nonlinear gain is implemented by a piecewise linear (PWL) function using a look-up table: $X = [0, 2.5, 3.5, 4, 4.49, 4.5]$; $Y = [10, 20, 40, 100, 200, 200]$.

The CCS nonlinear controller that uses a PWL nonlinear gain is shown in Fig. 15. The control gain has a nonlinear part (NG_{Ifc}, given by the PWL nonlinear gain) and a linear part (G_{Ifc}). The last part increases the mitigation performance by choosing a value in range 1–10. A higher value than 10 increases the switching frequency over to 50 kHz, so, G_{Ifc} value is set to 10.Designing of nonlinear law by a Fuzzy Logic Controller

If the used constant gain is $G_{Ifc} = 10$ and the Xg vector is the scaled X vector by this G_{Ifc} gain, then the nonlinear gain that includes this constant gain may be implemented by the following PWL function:

$$Xg = [0,\ 0.25,\ 0.35,\ 0.4,\ 0.449,\ 0.45];$$

$$Y = [10,\ 20,\ 40,\ 100,\ 200,\ 200].$$

The memberships functions for the fuel cell current ripple (fc), the ripple mitigation ratio (rm) and the command signal (com) are shown in Fig. 16, plot a, b and c, respectively. Five membership's functions are defined for both input variables in correlation with PWL vectors (Xg, Y). They are named as VS = Very Small, S = Small, M = Medium, B = Big and VB = Very Big. For output variable (com) are uniformly defined five membership's functions in range 0–1, too. They are also named as VS = Very Small, S = Small, M = Medium, B = Big and VB = Very Big. The base rules are shown in Fig. 16d. The Mamdani implication and center of gravity defuzzification method are used. The projections of contour (for the resulting control surface) are shown in Fig. 16e for different command signal levels.

It can be observed that projection contour for command signal level of 0.7 is similar with the shape of the PWL nonlinear gain that include the constant gain, $G_{Ifc} = 10$. So, the hysteresis levels can be chosen around this value. These results and simulation performed with FLC confirm the design made for the CCS nonlinear controller in the above section.Simulation results using a CCS nonlinear controller in mitigation control loop

Some simulation results are presented in Fig. 17 for the FC HPS topology with the CCS nonlinear controller that uses a PWL nonlinear gain. The 100 Hz harmonic level of fuel cell current (plot a), buck CCS current (plot b) and load current (showed in Fig. 8) are of 0.032 A, 7.357 A and 7.397 A, respectively. The ripple mitigation ratio is about $7.397/0.032 \cong 231$, and it is better than the result obtained by using a constant gain (see Fig. 14b). Comparing the LF power spectrums of buck CCS current and load current, it can be observed that are almost the same. Unfortunately, the HF power spectrum of the buck CCS current make its use (as one FLC input without prior processing) to be an impractical solution. So, a 1 ms

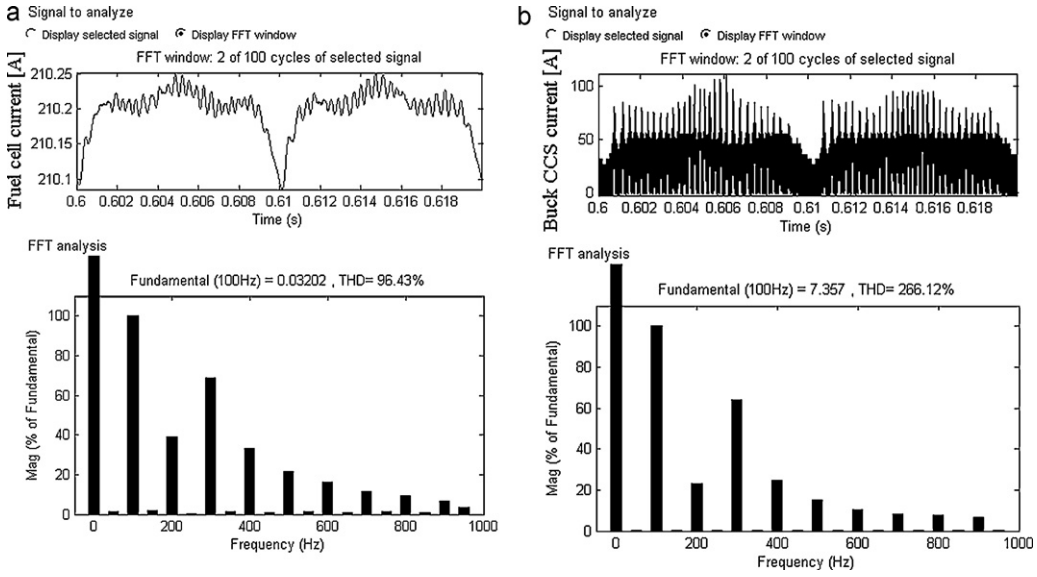


Fig. 17. Simulation results for FC HPS topology with nonlinear CCS controller. (a) Fuel cell current ripple (top) and its LF power spectrum (bottom). (b) Buck CCS current ripple (top) and its LF power spectrum (bottom).

moving-window means filter will be used for the signal processing of both FLC inputs. In this case the same delay will appear on both input variables.

The simulation results in case of CCS controller that uses a FLC are almost the same with those obtained above. If the moving-window of the mean filters is lager than 1 ms, then the delays in the processing of input variable will start to influence the mitigation performance.

8. Conclusion

In this paper the issue related to LF current ripple mitigation is presented step by step. The HPS topology of LF ripple mitigation by injection of an anti-ripple in the HPS output node was modeled and analyzed. The designing of an active control for real-time tracking of the LF ripple shape by a hysteretic control of buck CCS is presented here. Also, the designing of a dedicated nonlinear controller is presented step by step. Two ways to design of the nonlinear control law are proposed. The advantages of nonlinear controller are shown by computing the ripple mitigation ratio and ripple factor. Lower values of these performance indicators are obtained by a good designing of the nonlinear controller based on FLC.

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